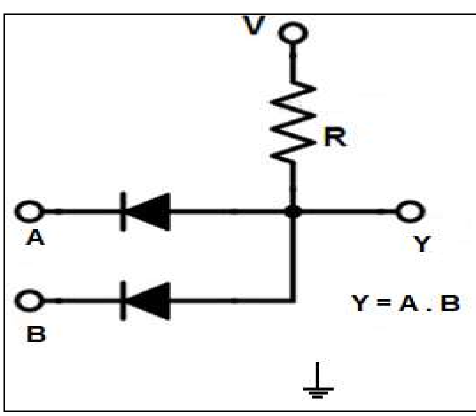
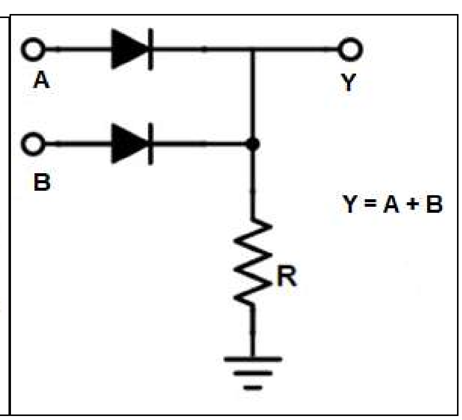
MODEL ANSWER

WINTER– 18 EXAMINATION

Subject Title: **Digital Techniques** **Subject Code:** 22320

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q. No.	Sub Q.N.	Answer	Marking Scheme
Q.1		**Attempt any FIVE of the following :**	**Total Marks 10**
	a)	**Write the radix of binary,octal,decimal and hexadecimal number system.**	**2M**
	Ans:	**Radix of: Binary – 2** **Octal - 8** **Decimal - 10** **Hexadecimal -16**	**½ M each**
	b)	**Draw the circuit diagram for AND and OR gates using diodes.**	**2M**
	Ans:	**Diode AND gate :Diode OR gate :** 	**1 M each**

c) **Write simple example of Boolean expression for SOP and POS.** **2M**

Ans:

SOP form:

$$Y = AB + BC + A\overline{C}$$

POS form:

$$Y = (A + B)(B + C)(A + \overline{C})$$

1 M each (any proper example can be considered)

d) **State the necessity of multiplexer.** **2M**

Ans:

Necessity of Multiplexer:

- It reduces the number of wires required to pass data from source to destination.
- For minimizing the hardware circuit.
- For simplifying logic design.
- In most digital circuits, many signals or channels are to be transmitted, and then it becomes necessary to send the data on a single line simultaneously.
- Reduces the cost as sending many signals separately is expensive and requires more wires to send.

2 M(any two proper points)

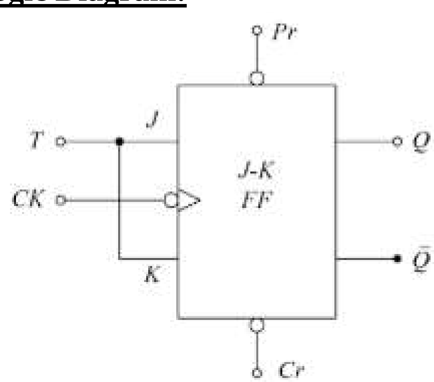
e) **Draw logic diagram of T flip-flop and give its truth table.** **2M**

Ans:

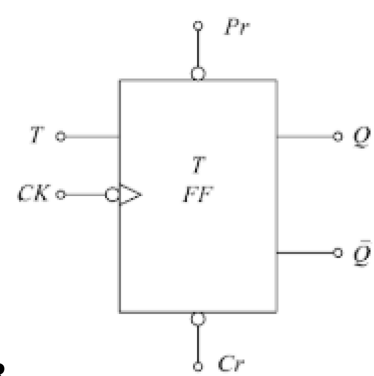
Note: Diagram Using logic gates with proper connection also can be consider.

1M (any one diagram)

Logic Diagram:



OR



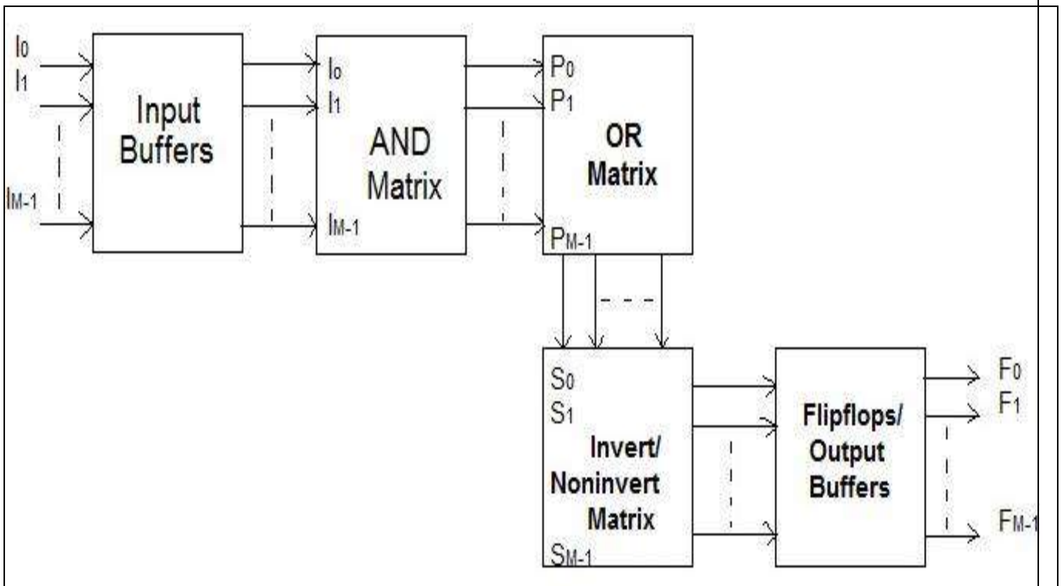
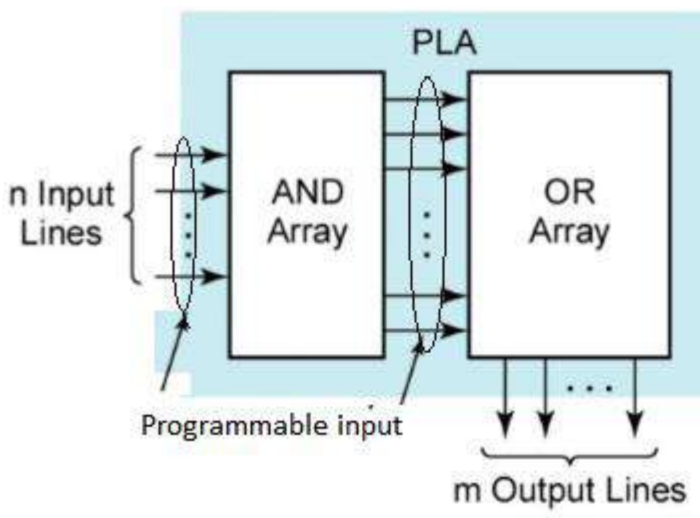
1 M

Truth Table:

Input T_n	Output Q_{n+1}	Operation Performed
0	Q_n	No change
1	$\bar{Q}_n$	Toggle

f)	**Define modulus of a counter. Write the numbers of flip flops required for Mod-6 counter.**	**2M**
Ans:	• Modulus of counter is defined as number of states/clock the counter countes. • The numbers of flip flops required for Mod-6 counter is 3.	**Definition: 1 M** **No. of FF- 1M**
g)	**State function of preset and clear in flip flop.**	**2M**
Ans:	• In the flip flop , when the power is switched on, the state of the circuit is uncertain i.e. may be Q = 1 or Q = 0. • Hence, the function of preset is to set a flip flop i.e. Q = 1andthe function of clear is to clear a flip flop i.e. Q = 0.	**1 M for each function (table is optional)**

Inputs			Output	Operation performed
CK	*Cr*	*Pr*	*Q*	
1	1	1	Q_{n+1}(Table 7.1)	Normal FLIP-FLOP
0	0	1	0	Clear
0	1	0	1	Preset

Q 2		**Attempt any THREE of the following :**	**12-Total Marks**
	a)	**Draw the block diagram of Programmable Logic Array.**	**4M**
	Ans:	**Diagram :-**  **Block diagram of Programmable Logic Array** **OR** 	**4 M**

b) **Convert –**
$(255)_{10}$ = $(?)_{16}$ = $(?)_8$
$(157)_{10}$ = $(?)_{BCD}$ = $(?)_{Excess3}$ — **4M**

Ans: **(i)** **$(255)_{10}$ = $(FF)_{16}$ = $(377)_8$**

$(255)_{10}$ = $(FF)_{16}$ — **1 M**

```
16 | 255    F (15)   ↑
   ------
   | 15     F
```

$(255)_{10}$ = $(377)_8$ — **1 M**

```
8 | 255     7   ↑
  ------
8 | 31      7
  ------
  | 3       3
```

(ii) **$(157)_{10}$ = $(000101010111)_{BCD}$ = $(010010001010)_{Excess3}$**

$(157)_{10}$ = $(000101010111)_{BCD}$ — **1 M**

```
  1    5    7
0001 0101 0111
```

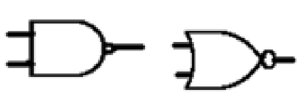
$(000101010111)_{BCD}$ = $(010010001010)_{Excess3}$ — **1 M**

```
   1 1   1 1 1  1 1 1
   0001 0101 0111
 + 0011 0011 0011
 ----------------
   0100 1000 1010
```

c) **Draw the symbol, truth table and logic expression of any one universal logic gate. Write reason why it is called universal gate.** — **4M**

Ans: ***(Note: Any one universal gate has to be considered.)***

Universal Gates: NAND or NORSymbol: — **1 M**



Truth table: — **1 M**

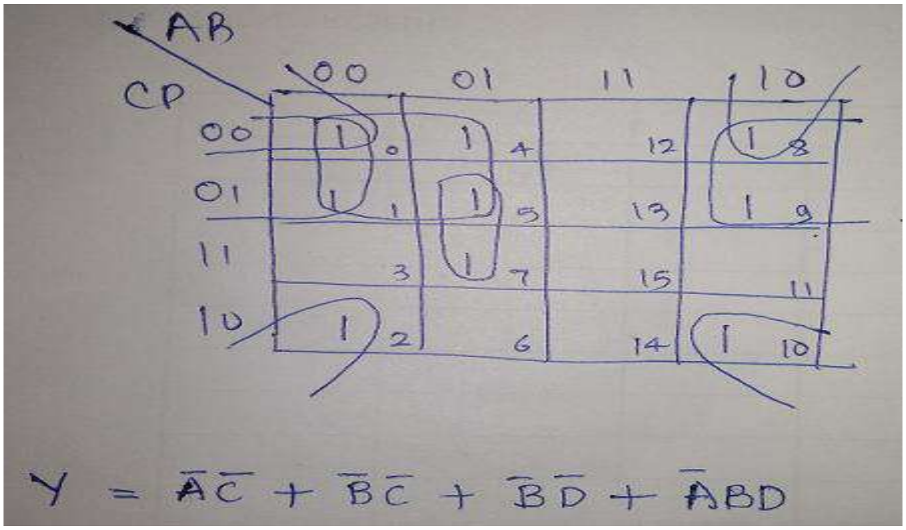
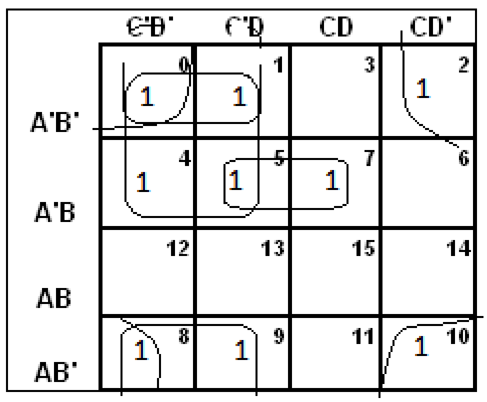
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Logic expression: — **1 M**

$Y = \overline{A \cdot B}$ $Y = \overline{(A + B)}$

NAND and NOR gates are called as "Universal Gate" as it is possible to implement any Boolean expression using these gates. — **1 M**

	d)	**Minimize the following expression using K-Map.** **$f(A, B, C, D) = \sum m(0, 1, 2, 4, 5, 7, 8, 9, 10)$**	**4M**
	Ans:	 OR  $\bar{A}\bar{C} + \bar{B}\bar{C} + \bar{B}\bar{D} + \bar{A}BD$	**1 M – drawing k map** **1 M – Representing function in k map** **1 M – Grouping** **1M – Final expression**

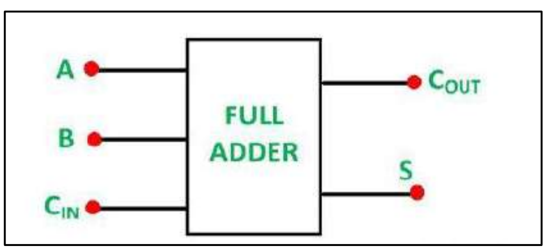
Q. 3		**Attempt any THREE:**	**12-Total Marks**
	a)	**Compare TTL and CMOS logic families on the basis of following:** **(i) Propagation delay** **(ii) Power Dissipation** **(iii) Fan-out** **(iv) Basic gate**	**4M**
	Ans:	***NOTE :- (Relevant points of comparison- 1 M for each point)***	**1 Marks each point**

Parameter	**CMOS**	**TTL**
Propagation delay	70-105 nsec/more than TTL	10 nsec/Less than CMOS
Power Dissipation	Less 0.1 mW/Less than TTL	More 10 mW/ More than CMOS
Fan-out	50/More than TTL	10/Less than CMOS
Basic gate	NAND/NOR	NAND

	b)	**Describe the function of full Adder Circuit using its truth table, K-Map simplification and logic diagram.**	**4M**
	Ans:	**(Diagram- 1M,Truth table-1M, K-map- 1M,Logic diagram-1 M)**	

A full adder is a combinational logic circuit that performs addition between three bits, the two input bits A and B, and carry C from the previous bit.

Block diagram : **1M**



1M

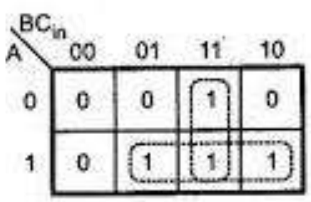
Truth Table :

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

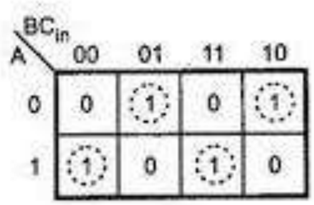
1M

K-Map :-

For Carry (C_{out})



For Sum



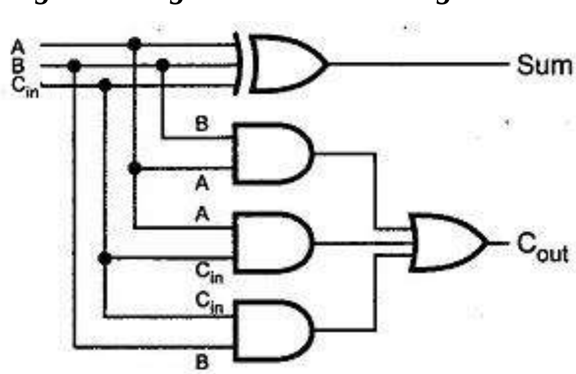
$C_{out} = AB + A\,C_{in} + B\,C_{in}$

$Sum = \overline{A}\,\overline{B}C_{in} + \overline{A}B\overline{C}_{in} + A\overline{B}\,\overline{C}_{in} + ABC_{in}$

1M

Logic Diagram:

(Note: Logic Diagram using basic or universal gate also can be consider)



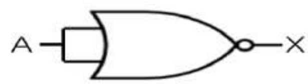
$A \oplus B) \oplus C_{in}$

: $(AB + AC_{in} + BC_{in})$

c) **Realize the basic logic gates, NOT, OR and AND gates using NOR gates only.** **4M**

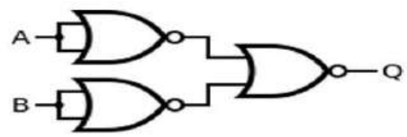
Ans:

(NOT GATE USING NOR GATE:1 M) **1M**



where, X = A NOR A
$x = \bar{A}$

(AND GATE USING NOR GATE:1.5 MARKS)

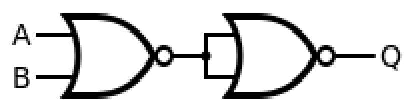


1.5M

$Q = \overline{\bar{A} + \bar{B}} = \bar{A} + \bar{B}$

$= \overline{\overline{A.B}}$
= A.B

(OR GATE USING NOR GATE:1.5 MARKS)



1.5 M

$Q = \overline{\overline{A+B}}$
=A+B

d) **Describe the working of JK flip-flop with its truth table and logic diagram.** **4M**

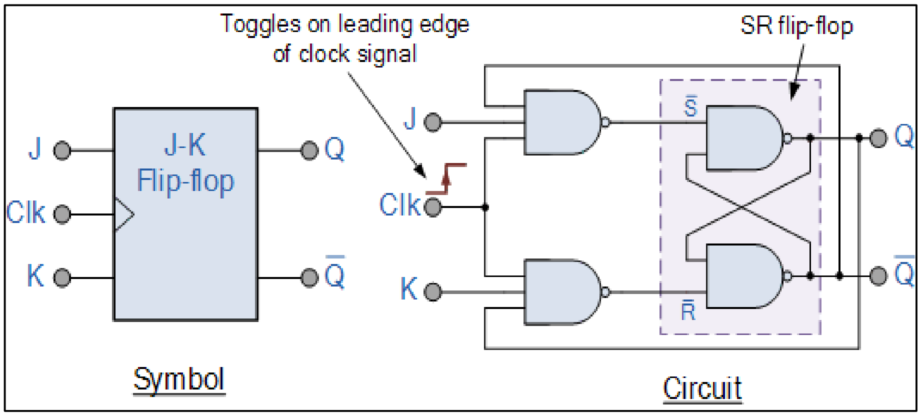
Ans: ***(Diagram-2 M,Working-1M,Truth table-1M)***

Truth Table :- **1M**

Truth Table

J	K	CLK	Q
0	0	↑	Q_0(no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q}_0$ (toggles)

Diagram :-



2M

Working :-

The **JK flip flop** is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level "1". Due to this additional clocked input, a JK flip-flop has four possible input combinations, "logic 1", "logic 0", "no change" and "toggle". **1M**

Both the S and the R inputs of the previous SR bistable have now been replaced by two inputs called the J and K inputs, respectively after its inventor Jack Kilby. Then this equates to: J = S and K = R.

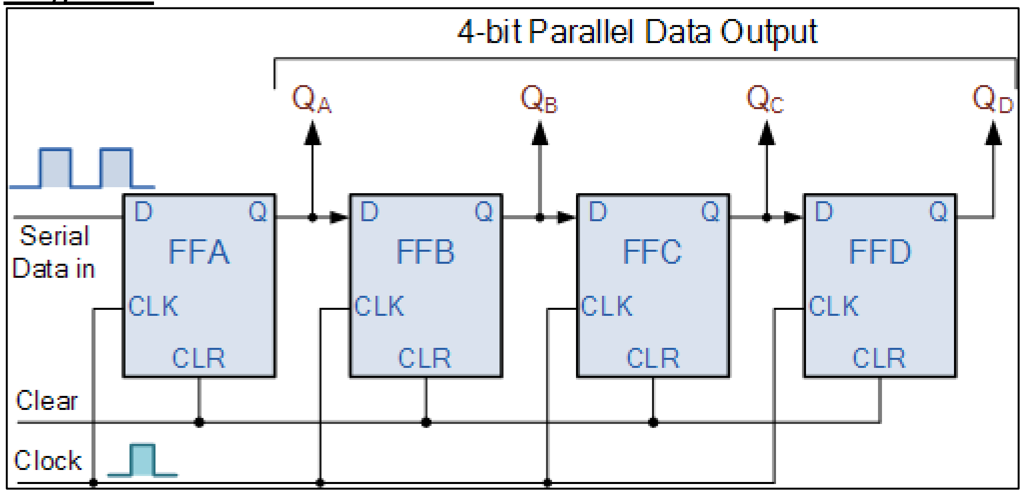
The two 2-input AND gates of the gated SR bistable have now been replaced by two 3-input NAND gates with the third input of each gate connected to the outputs at Q and Q. This cross coupling of the SR flip-flop allows the previously invalid condition of S = "1" and R = "1" state to be used to produce a "toggle action" as the two inputs are now interlocked.

If the circuit is now "SET" the J input is inhibited by the "0" status of Q through the lower NAND gate. If the circuit is "RESET" the K input is inhibited by the "0" status of Q through the upper NAND gate. As Q and Q are always different we can use them to control the input. When both inputs J and K are equal to logic "1", the JK flip flop toggles

Q. 4	**A)**	**Attempt any THREE of the following:**	**12-Total Marks**
	a)	**Draw and explain working of 4 bit serial Input parallel Output shift register.**	**4M**

Ans: **(Diagram:2M,Explaination:2M)**

<u>Diagram :-</u> **2M**



<u>Explaination :-</u> **2M**

If a logic “1” is connected to the DATA input pin of FFA then on the first clock pulse the output of FFA and therefore the resulting Q_A will be set HIGH to logic “1” with all the other outputs still remaining LOW at logic “0”. Assume now that the DATA input pin of FFA has returned LOW again to logic “0” giving us one data pulse or 0-1-0.

The second clock pulse will change the output of FFA to logic “0” and the output of FFBand Q_B HIGH to logic “1” as its input D has the logic “1” level on it from Q_A. The logic “1” has now moved or been “shifted” one place along the register to the right as it is now at Q_A.

When the third clock pulse arrives this logic “1” value moves to the output of FFC (Q_C) and so on until the arrival of the fifth clock pulse which sets all the outputs Q_A to Q_D back again to logic level “0” because the input to FFA has remained constant at logic level “0”.

The effect of each clock pulse is to shift the data contents of each stage one place to the right, and this is shown in the following table until the complete data value of 0-0-0-1 is stored in the register. This data value can now be read directly from the outputs of Q_A to Q_D.

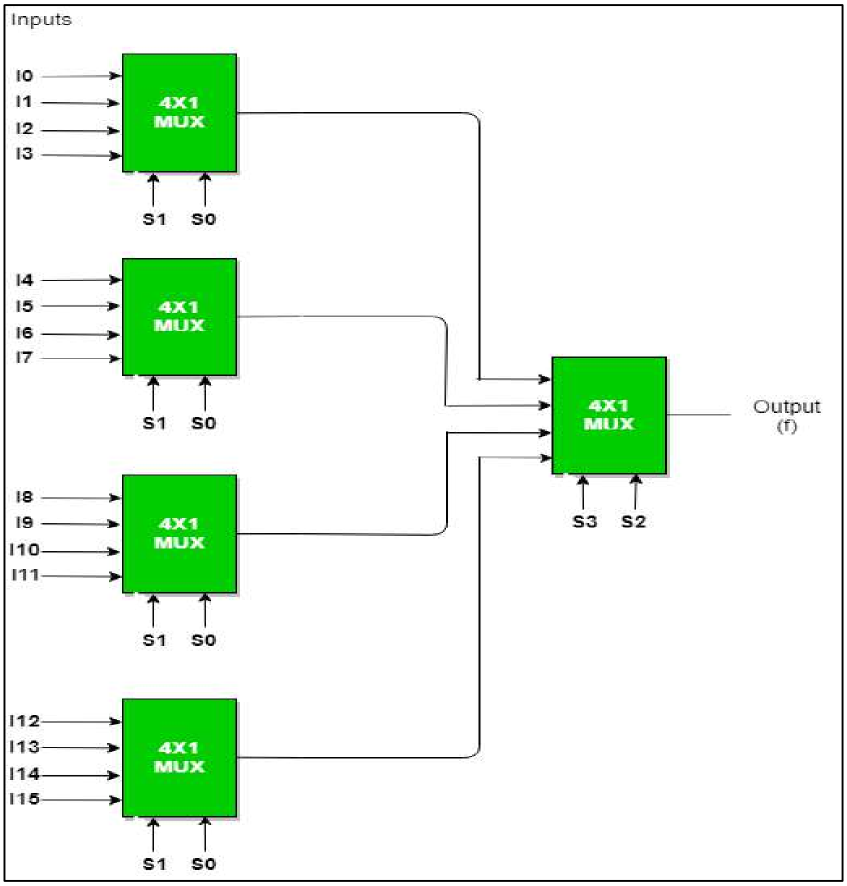
Then the data has been converted from a serial data input signal to a parallel data output. The truth table and following waveforms show the propagation of the logic “1” through the register from left to right as follows.

Basic Data Movement Through A Shift Register

Clock Pulse No	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	0	0	0	0

b) **Draw 16:1 MUX tree using 4:1 MUX.** **4M**

Ans: **<u>Diagram :-</u>**



4M

	c)	**Calculate analog output of 4 bit DAC for digital input 1101.** **Assume V_{FS} = 5V.**	**4M**
	Ans:	**(Formula- 1M, Correct problem solving- 3M)** **<u>Formula :-</u>** **$V_R = V_{FS}$** $V_o = V_R [d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}]$ $= 5(1x2^{-1} + 1x2^{-2}+0x2^{-3}+1x2^{-4})$ = 5(0.5+O.25+0+0.0625) = 4.0625 Volts **OR** $V_{FS} = V_R . (\frac{b3}{2} + \frac{b2}{4} + \frac{b1}{8} + \frac{b0}{16})$ Note – (Since V_R is not given find **V_R)** Full Scale o/p mean b3 b2 b1 b0 = 1111 V_{FS} = 5V $5 = V_R . (\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16})$ **V_R = 5.33** For digital i/p b3 b2 b1 b0 = 1101 $V_0 = 5.33 (\frac{1}{2} + \frac{1}{4} + \frac{0}{8} + \frac{1}{16})$ **V_0 = 4.33V**	**1M** **3M** **2 Marks for V_R and 2 marks for V_o**
	d)	**State De Morgan's theorem and prove any one.**	**4M**
	Ans:	**(Each State and proof using table- 2M each)**	**2M**

i) $\overline{AB} = \overline{A} + \overline{B}$

It states that compliment of product is equal to sum of their compliments.

1	2	3	4	5	6
A	B	$\overline{AB}$	$\overline{A}$	$\overline{B}$	$\overline{A}+\overline{B}$
0	0	1	1	1	1
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	0	0	0

Column 03 = column 06

i.e. $\overline{AB} = \overline{A}+\overline{B}$

Hence proved

2M

OR

ii) $\overline{A+B} = \overline{A} \cdot \overline{B}$

It states that complement of sum is equal to product of their complements.

1	2	3	4	5	6
A	B	$\overline{A+B}$	$\overline{A}$	$\overline{B}$	$\overline{A}\cdot\overline{B}$
0	0	1	1	1	1
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	0

Column 03 = column 06

$\therefore\ \overline{A+B} = \overline{A}\cdot\overline{B}$

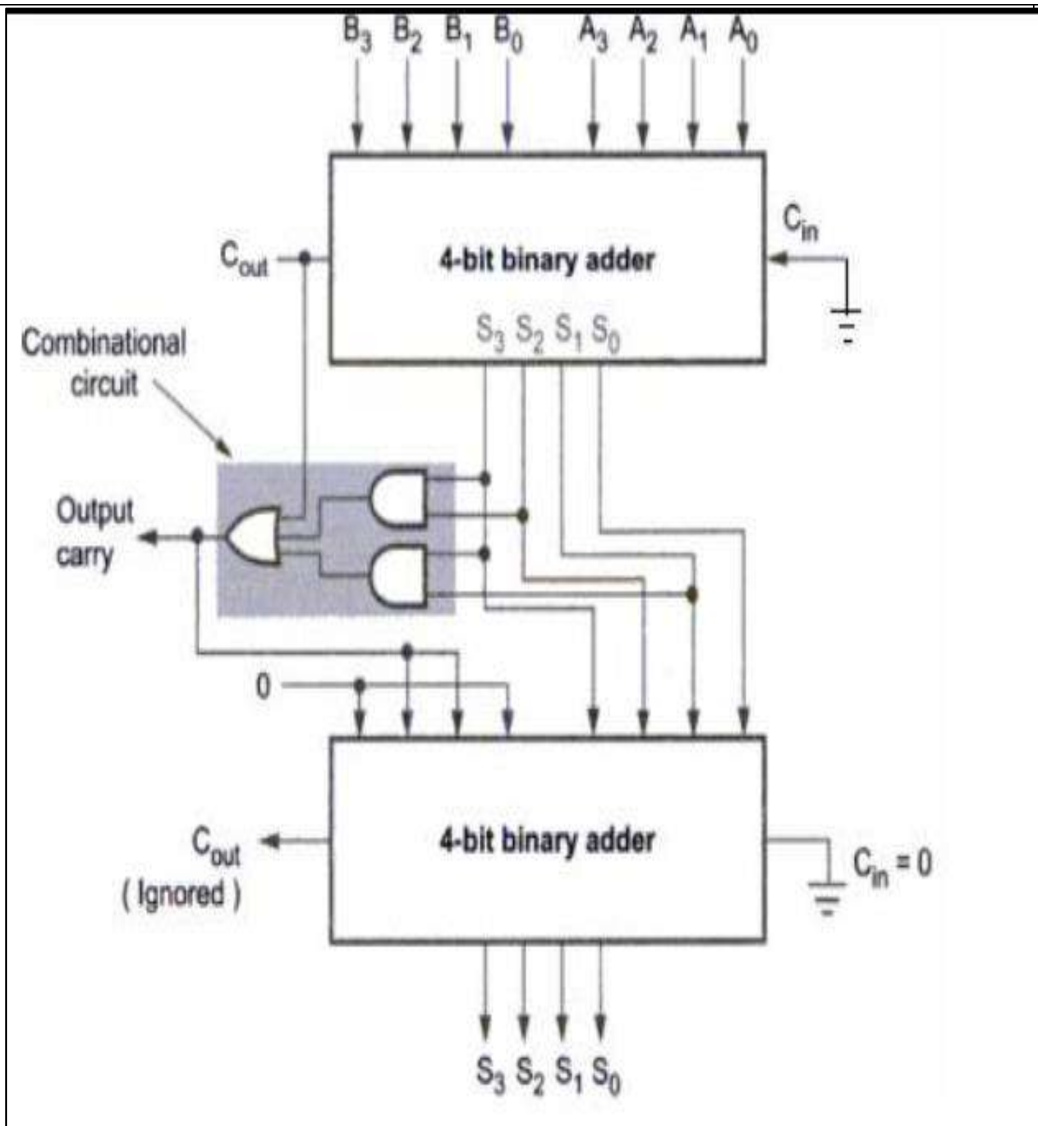
Hence proved.

e) **Design one digit BCD Adder using IC 7483**

Ans: **(Diagram:4M)**

(Note: Labeled combinational circuit can be drawn using universal gate also)

4M



Q.5		**Attempt any TWO of the following :**	**Total Marks 12**
	a)	**Subtract using 2's compliment method** **$(35)_{10} – (5)_{10}$**	**6M**
	Ans:	Step 1 – Obtain binary equivalent of $(35)_{10}$& $(5)_{10}$ & then take 2's compliment of $(5)_{10}$. i.e. $(35)_{10} = (100011)_2$ $(5)_{10} = (101)_2$ 2's compliment of $(5)_{10} = (000101)_2 =$ 111010 → 1's compliment + 1 --------------------------------- $(111011)_2$→ 2's Compliment Step -2 :	**Each step 3 Marks**

Now add $(100011)_2$ and $(111011)_2$

```
          100011
       +  111011
-----------------------------
 [1]     011110
```

→ Carry is generated so answer is in positive form, so will discard the carry generated

Therefore final answer will be **$(011110)_2 = (30)_2$**

b) **Design a 4 bit synchronous counter and draw its logic diagram.** **6M**

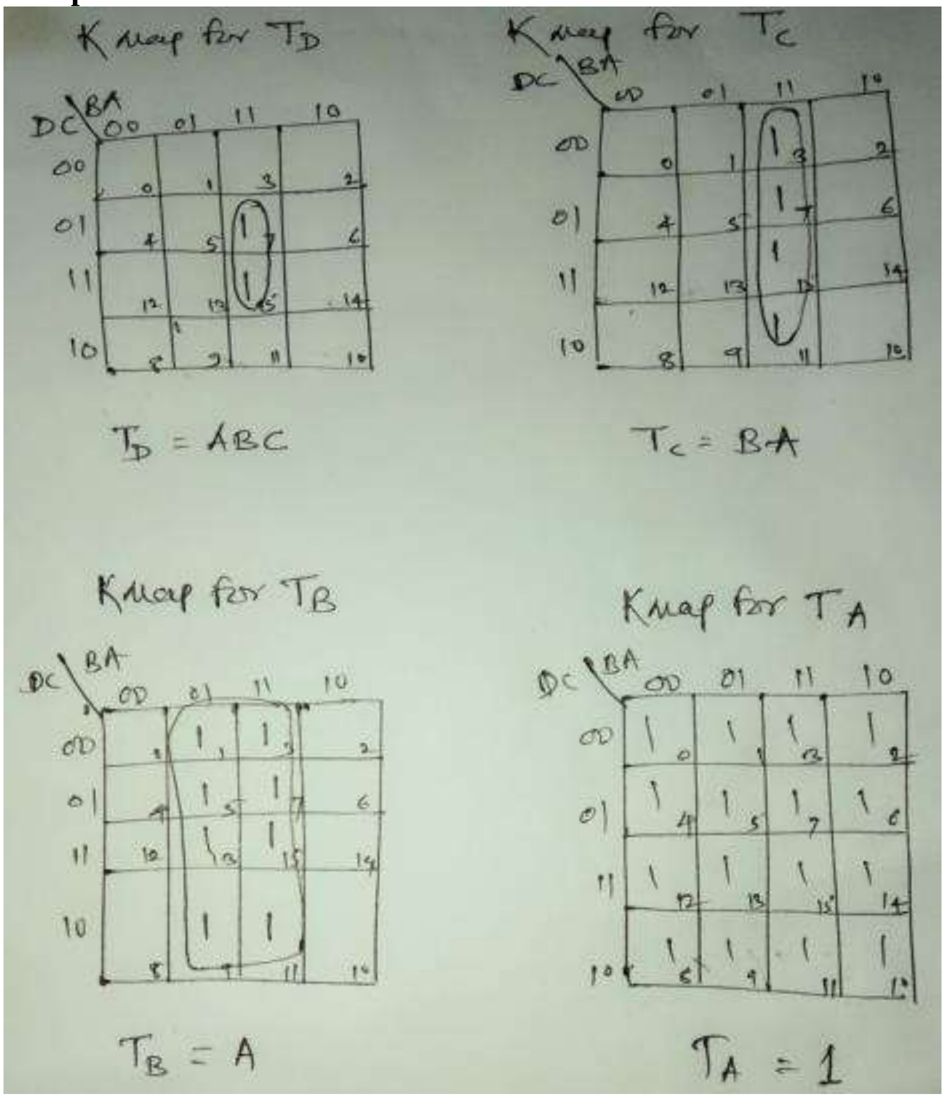
Ans: **State Table:**

Present state				Next state				Flip flop inputs			
D	C	B	A	D^+	C^+	B^+	A^+	T_D	T_C	T_B	T_A
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	1
0	1	0	1	0	1	1	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	1
0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	1
1	0	0	1	1	0	1	0	0	0	1	1
1	0	1	0	1	0	1	1	0	0	0	1
1	0	1	1	1	1	0	0	0	1	1	1
1	1	0	0	1	1	0	1	0	0	0	1
1	1	0	1	1	1	1	0	0	0	1	1
1	1	1	0	1	1	1	1	0	0	0	1
1	1	1	1	0	0	0	0	1	1	1	1

2M-State table

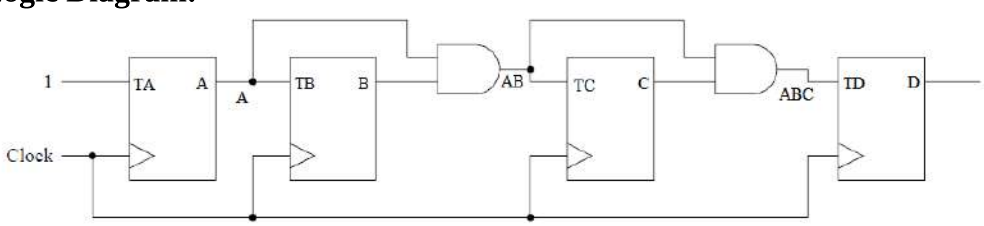
Kmap:

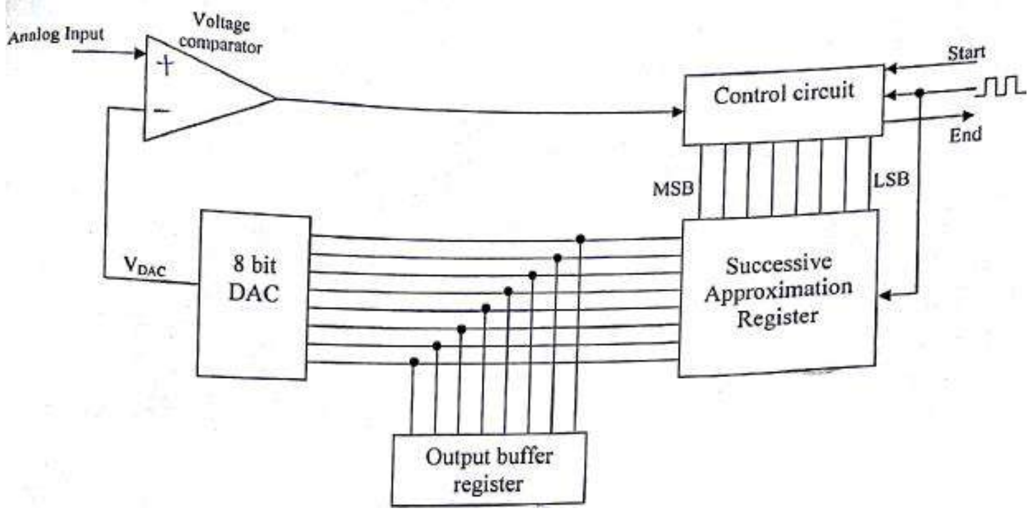
2M-Kmap



Logic Diagram:

2M-Logic Diagram

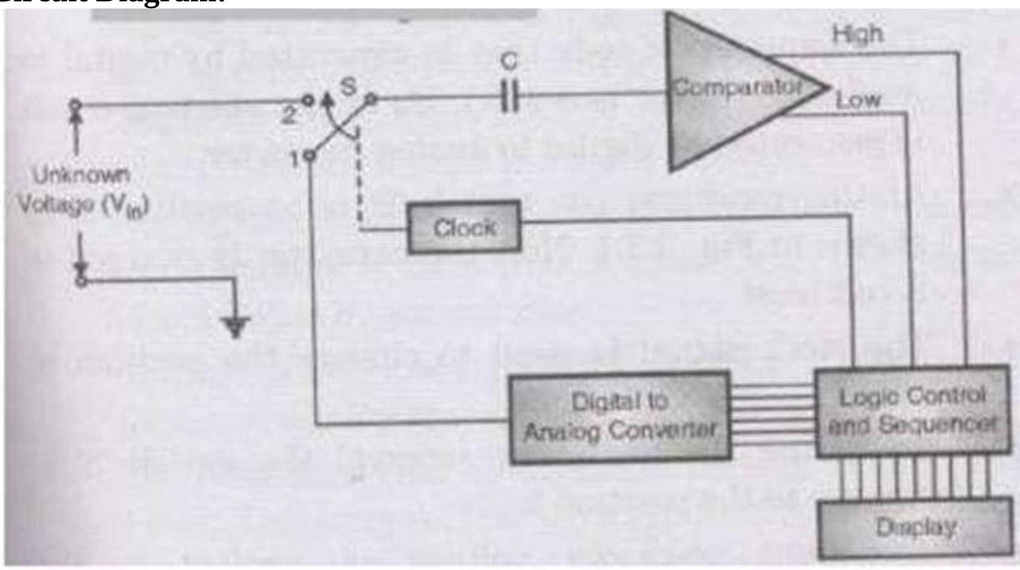


	c)	**Describe the working of Successive Approximation ADC. Define Resolution and conversion time associate with ADC.**	**6M**
	Ans:	**Circuit Diagram:**  When the start signal goes low the successive approximation register SAR is cleared and output voltage of DAC will be 0V. When start goes high the conversion starts. After starts, during first clock pulse the control circuit set MSB bit so SAR output will be 1000 0000. This is connected as input to DAC so output of DAC is (analog output) compared with V_{in} input voltage. If V_{DAC} is more than V_{in} the comparator output $-V_{sat}$, if V_{DAC} is less than $V_{in,}$ the comparator output is $+V_{sat.}$ If output of DAC i.e. V_{DAC} is $+ V_{sat}$ (i.e unknown analog input voltage $V_{in} > V_{DAC}$) then MSB bit is kept set, otherwise it is reset. Consider MSB is set so SAR will contain 1000 0000. The next clock pulse will set next bit i.e D_6 a digital output of 1100 0000. The output voltage of DAC i.e V_{DAC} is compared with V_{in}, if it is $+ V_{sat}$the D_6 bit is kept as it is, but if it is $-V_{sat}$ the D_6 bit reset. The process of checking and taking decision to keep bit set or to reset is continued upto D_0. Then the DAC input will be digital data equal to analog input. When the conversation if finished the control circuits sends out an end of conversion signal and data is locked in buffer register	2 Marks Diagram 2 Marks Explanation 1 Marks Each

Resolution: The voltage input change necessary for a one bit change in the output is called resolution.
Conversion Time: The conversion time is the time required for conversion from an analog input voltage to the stable digital output

OR

Circuit Diagram:



2 Marks Diagram

Explanation:

2 Marks Explanation

DAC= Digital to Analog converter
EOC= End of conversion
SAR =Succesive approximation register
S/H= Sample and hold circuit
Vin= input voltage
Vref= reference voltage
The successive approximation Analog to Digital converter circuit typically consisting of four sub circuits-
1. A sample and hold circuit to acquire the input voltage Vin.
2. An analog voltage comparator that compares Vin to the output of internal DAC and outputs the result of comparison to successive approximation register(SAR).
3. SAR sub circuits designed to supply an approximate digital code of Vin to the internal DAC.
4. An internal reference DAC that supplies the comparator with an analog voltage equivalent of digital code output of SAR for comparison with Vin.

The successive approximation register is initialized so that most significant bit (MSB) is equal to digital 1. This code is fed into DAC which the supplies the analog equivalent of this digital code Vref/2 into the comparator circuit for the comparison with sampled input voltage. If this analog voltage exceeds Vin the comparator causes the SAR to reset the bit, otherwise a bit is left as 1. Then the next bit is set to 1 and the same test is done continuing this binary search until every bit in the SAR has been tested. The resulting code is the digital approximation of the sampled input voltage and is finally output by DAC at end of the conversion (EOC).

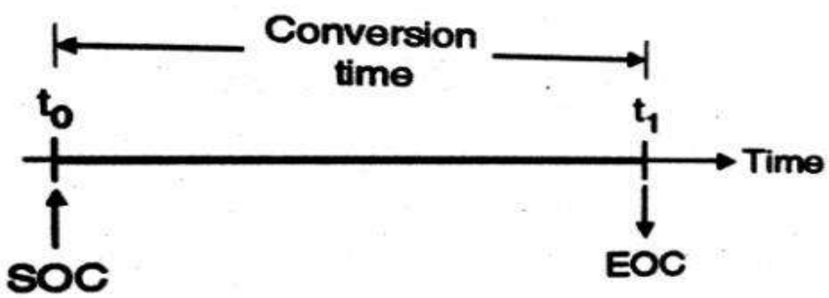
Resolution and conversion time associate with ADC-

Resolution:
It is the maximum number of digital output codes.
Resolution= 2^n
(OR)
It is defined as the ratio of change in the value of input analog voltage required to change the digital output by 1 LSB.

1 Marks each

$$\therefore \text{Resolution} = \frac{V_{FS}}{2^n - 1}$$

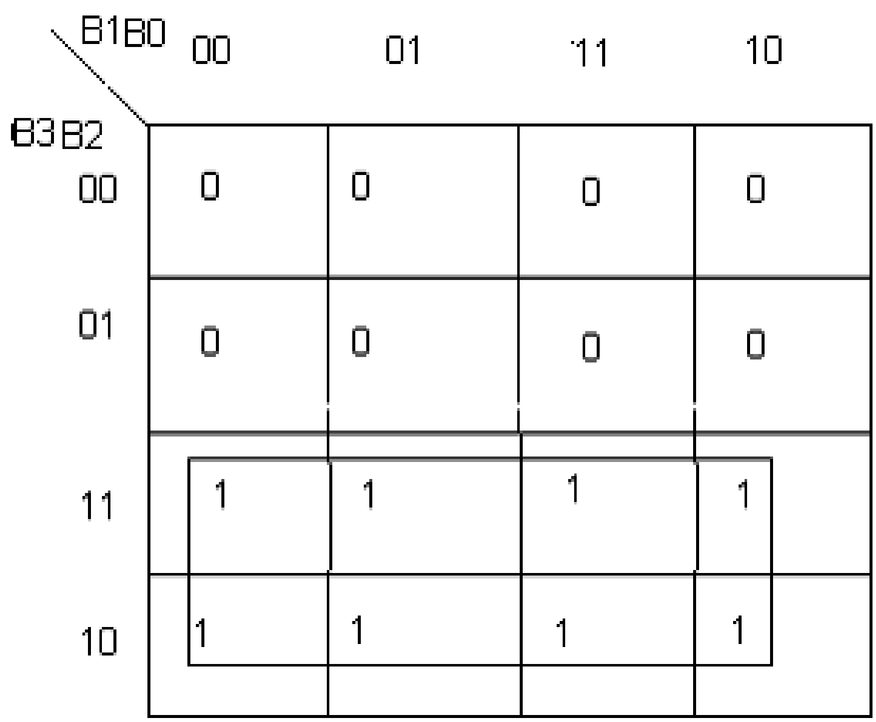
Conversion time:
The time difference between two instants i.e. 'to' where SOC signal is given as input to the ADC and 't1' where EOC signal we get as output from ADC. it should be small as possible.



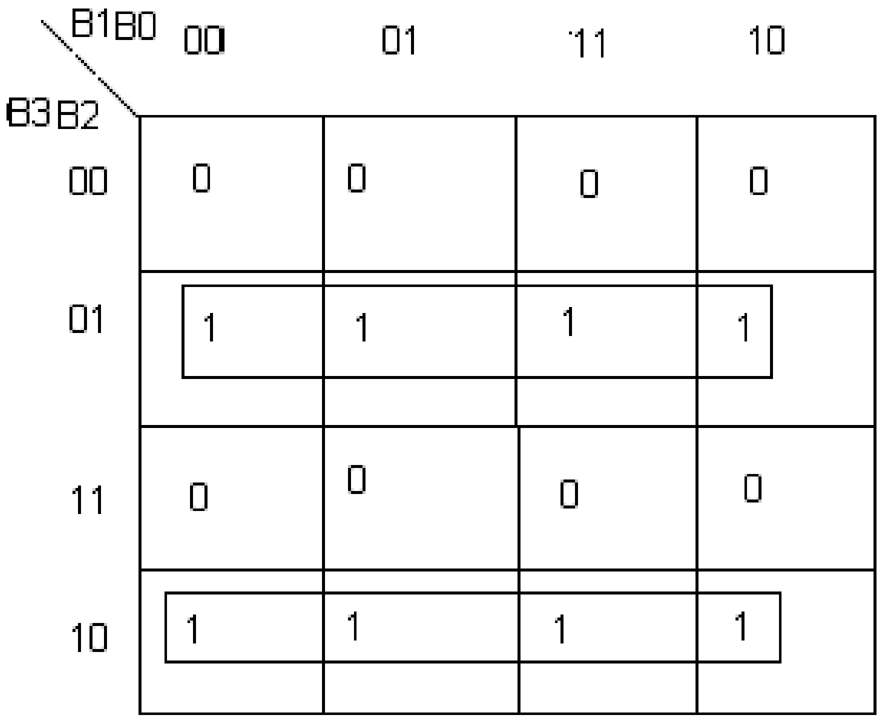
Q.6		**Attempt any TWO of the following:**	**Total Marks 12**
	a)	**Design 4 bit Binary to Gray code converter.**	**6M**
	Ans:	Truth Table for 4 bit Binary to Gray code converter	**2M for truth table** **1/2m for each output equation** **2M for realization using gates**

Binary Input				**Gray output**			
B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

K-MAP FOR G3:



G3=B3

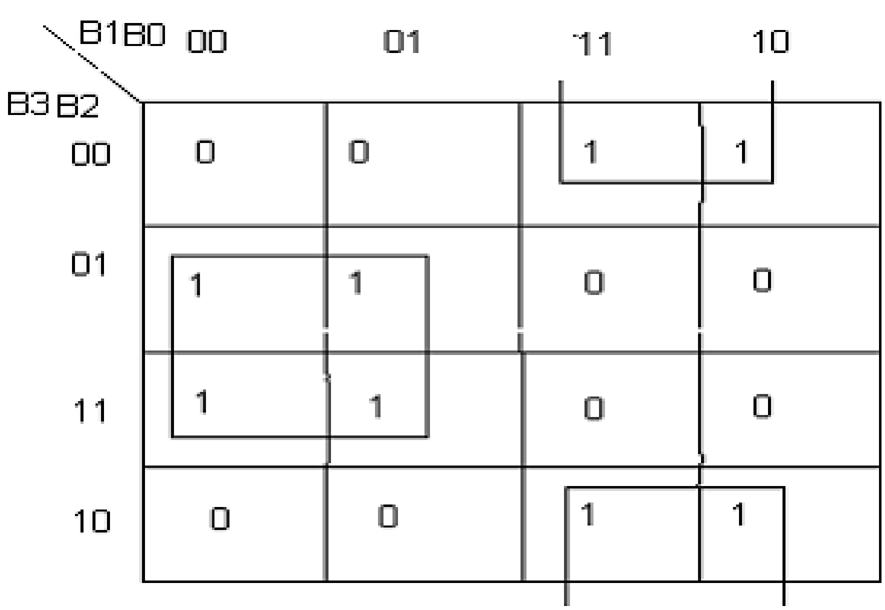


K-MAP FOR G2:

$G2=\overline{B3}\,B2+\overline{B2}\,B3$

= B3 XOR B2

K-MAP FOR G1:



$G1 = \overline{B2}\,B1 + B2\,\overline{B1}$

= B1 XOR B2

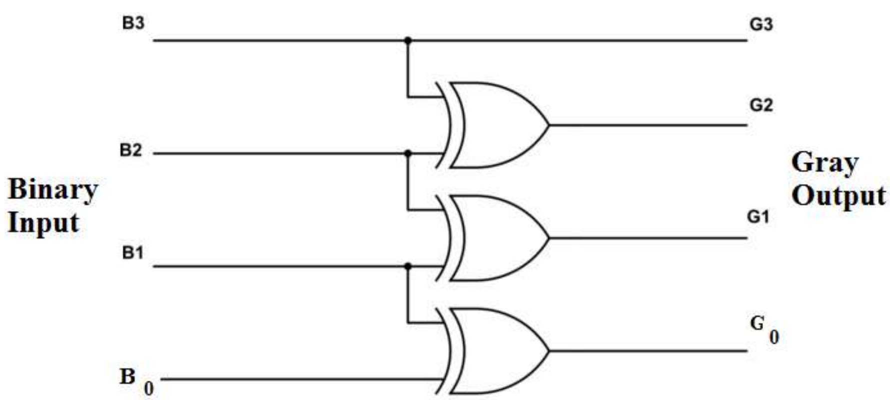
K-MAP FOR G0:

B3B2 \ B1B0	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	0	1	0	1
10	0	1	0	1

$G0 = \overline{B1}B0 + B1\overline{B0}$

= B1 XOR B0

Diagram for 4 bit Binary to Gray code converter:



Note: Realization of output equations can be done using Basic or Universal gates

	b)	**Compare the following (Any three points)** **i) Volatile with Non-volatile memory** **ii) SRAM with DRAM memory**	**6M**
	Ans:	(tables below)	**Any 3points (each 1 mark)**

Parameter	**Volatile memory**	**Non-Volatile memory**
definition	Memory required electrical power to keep information stored is called volatile memory	Memory that will keep storing its information without the need of electrical power is called nonvolatile memory.
classification	All RAMs	ROMs, EPROM, magnetic memories
Effect of power	Stored information is retained only as long as power is on.	No effect of power on stored information
applications	For temporary storage	For permanent storage of information

2. SRAM with DRAM memory

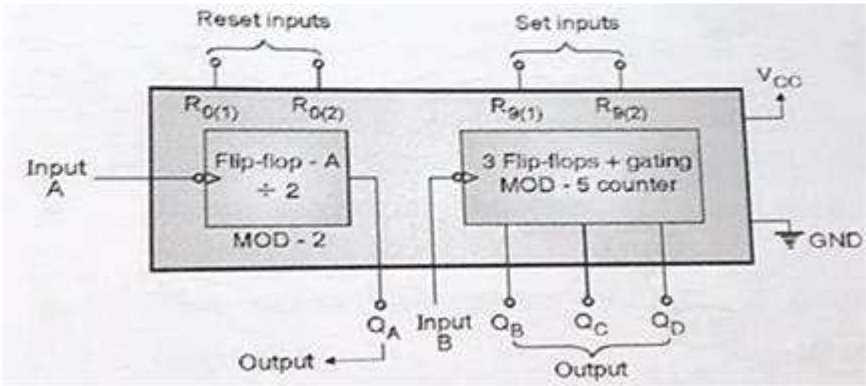
Parameter	**SRAM**	**DRAM**
Circuit configuration	Each SRAM cell is a flip flop	Each cell is one MOSFET & a capacitor
Bits stored	In the form of voltage	In the form of charges
No of components per cell	More	Less
Storage capacity	Less	More
Refreshing	It does not require refreshing	It require refreshing.
Cost	It is expensive	It is cheaper
Speed	It is faster	It is slower comparatively

c) **Give block schematic of decade counter IC 7490. Design Mod-7 counter using this IC.** **6M**

Ans:

1. block schematic of decade counter IC 7490-

2M block schematic



Mod-7 means states are from o,1,2,3,4,5,6,0
Therefore we have to reset counter IC 7490 when Q_D,Q_C,Q_B,Q_A=0111
Design reset logic:
Output of reset circuit should be HIGH because R0(1) and R0(2) are active high inputs.
Therefore reset logic output should be low for states 0 to 6.

Output should be HIGH for states 7 onwards.

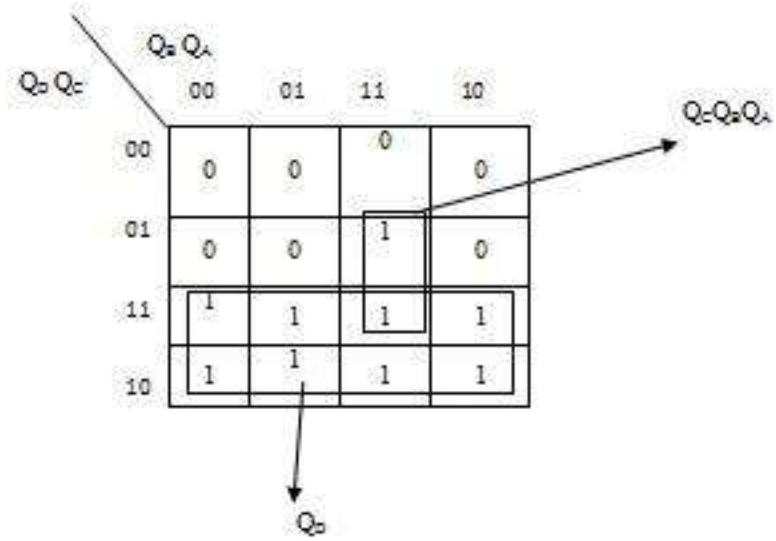
Truth table & K-map:

Q_D	Q_C	Q_B	Q_A	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1

Invalid State

Truth Table-1M
Kmap-1M
Logical Dig-2M

For Y



Expression for Y:

$$Y = Q_C\, Q_B\, Q_A + Q_D$$

Circuit is-

Logic Diagram: